D. Remarks

Objections to the Specification

Claim 20 has been amended to address this objection.

Rejection of Claims 1-3, 6-7, 17-19, and 22-24 Under 35 U.S.C. §103, based on *Hung et al.* (U.S. Patent Publication No. US2002/0132403 A1) in view of *Kim et al.* (U.S. Patent Publication No. US2002/0001935).

The rejection of claims 1-3 and 6-7 will first be addressed.

The semiconductor device of amended claim 1 includes an insulated gate field effect transistor (IGFET). A gate electrode of the IGFET includes a lower layer electrode formed on a gate insulating film and an upper layer electrode formed on the lower layer electrode. A cap film is formed on the upper layer electrode. A first nitride film is on a side surface of the upper layer electrode. The first nitride film has a film thickness of approximately 2 to 5 nm and does not cover the side surface of the cap film. The IGFET includes an oxide film on a side surface of the lower electrode and an etching stopper film including a second nitride film formed on the outside of the first nitride film and an outside surface of the oxide film.

As is well known, in proceedings before the Patent and Trademark Office, the examiner bears the burden of establishing a prima facie case of obviousness based on the prior art.[1]

To establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[2]

Applicant first traverses this rejection by noting the necessary motivation to combine for a prima facie case does not exist. The base reference *Hung et al.* teaches away from the proposed modification, as recognized by the Examiner in the previous Final Office Action.

The rejection notes that *Hung et al.* does not show that a "first nitride film... does not cover the side surface of the cap film". To show such a limitation, the rejection proposes modifying *Hung et al.* in view of *Kim et al.* according to the following rationale:

[1] Ex parte Obukowicz, 27 USPQ 1063, 105 (B.P.A.I. 1992).
[2] MPEP §2143.

> [I]t would have been obvious... to use the nitride film 25 teaching of Kim with Hung's device because it would have prevented transformation of the gate as taught by Kim..." (Office Action, dated 7/26/2005, Page 3, Last full paragraph).

The "transformation" being prevented by *Kim et al.* is the formation of oxide on a side surface of a gate layer (tungsten):

> In the re-oxidation process... a tungsten ***oxide***(WO_3) layer 200 ***is formed*** on the side walls of the gate electrode 100.... thereby deteriorating reliability of device. (*Kim et al.*, Paragraph [0008]).

Thus, as explicitly noted in the reference, the nitride film 25 of *Kim et al.* is for preventing an oxide on the side walls of a gate electrode.

> According to the present invention, oxidation of a tungsten layer is hindered from re-oxidation process, thereby preventing transformation of the gate electrode. (*Kim et al.*, Paragraph [0034]).

Thus, the rejection proposes including a nitride layer 25 of *Kim et al.* to prevent the formation of an oxide on a side surface of a gate electrode in *Hung et al.*

This reasoning cannot be sufficient for a prima facie case of obviousness as it directly contradicts the teachings of *Hung et al.* as recognized by the Examiner.

As understood from the above, the rejection argues that one skilled in the art would include a nitride layer 25 (from *Kim et al.*) to prevent oxidation of a gate electrode of *Hung et al.* However, in the previous Final Office Action, the Examiner explicitly admitted that no oxide is formed on the side surface of the gate electrode in *Hung et al.*:

> The Applicant pointed out... layer 10 of Hung at least covering the bottom of the side surface of silicide layer 6a as shown in Fig. 5. This is not persuasive because the layer 10 ***is not covering the bottom of the side surface of the silicide layer 6a***... A clearer indication ... is in fig. 3 oxide layer 9 on a side surface of the first lower gate electrode 5 ***and not on the side surface of the first upper layer gate***

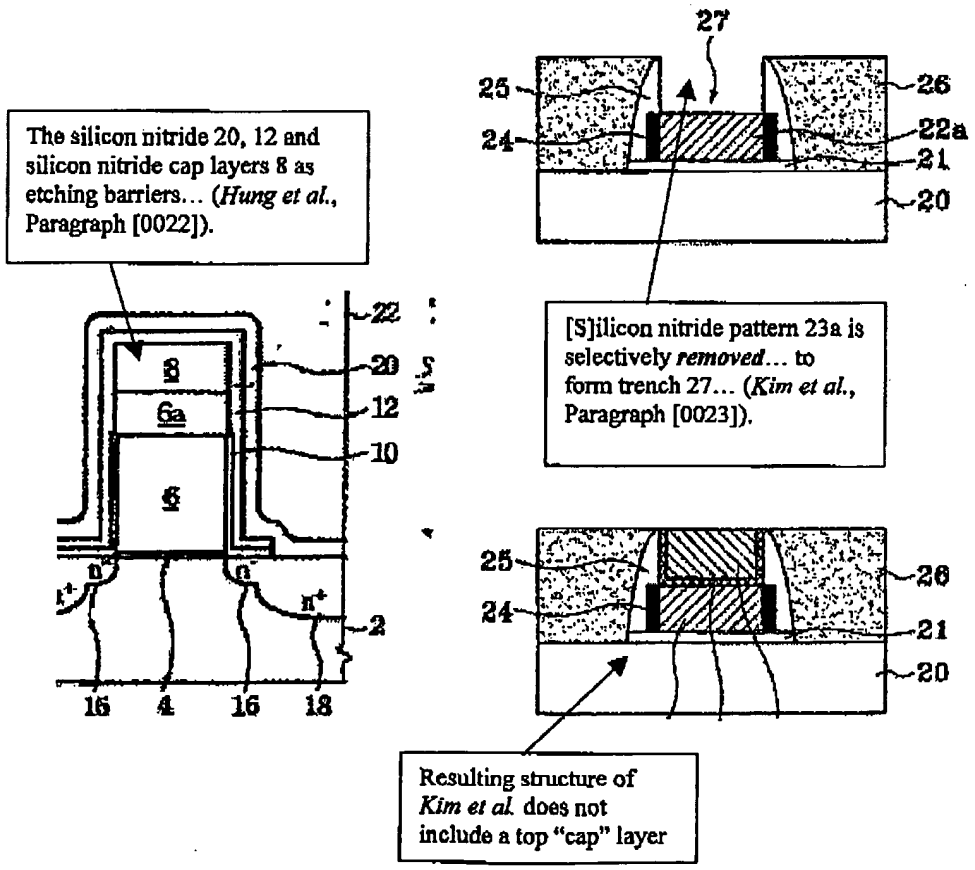
electrode 5a. (Final Office Action, dated 05/13/2005, Page 7, Line 17 to Page 8, Line 3).

That is, the rejection proposes a modification to address a problem that is admitted not to exist.

Accordingly, because the reference *Hung et al.* teaches away from the proposed modification, and thus necessary motivation for a prima facie case of obviousness does not exist.

Second, the necessary motivation for the proposed modification is further believed to be lacking as the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, or would change the principle operation of the prior art invention being modified.[3]

The gate structure of the reference being modified, *Hung et al.* includes a nitride cap layer 8 that functions as an etching barrier. The nitride layer 25 of *Kim et al.* that the rejection proposes incorporating into the structure of *Hung et al.* necessarily removes a top nitride layer to provide a trench in which to form a tungsten layer:



[3] See In re Gordon, 221 USPQ 1125 (Fed. Cir. 1984).

Thus, incorporating the nitride layer 25 of *Kim et al.* would eliminate the etch protection of a cap layer present in *Hung et al.*, rendering the resulting combination unsatisfactory for its intended purpose, or would change the principle operation.

For this additional reason, a prima facie case of obviousness it not believed to have been established.

The rejection of claims 17-19 will now be addressed.

The semiconductor device of claim 17 includes a first region and a second region. A first gate electrode of a first IGFET in the first region has a first lower layer electrode formed on a first gate insulating film and a first upper layer electrode formed on the first lower layer electrode. A first cap film is formed on the first upper layer electrode. A first nitride film is on a side surface of the first upper layer electrode that does not cover the side surface of the first cap film. A first oxide film is on a side surface of the first lower layer electrode. A first etching stopper film includes a second nitride film formed on the outside of the first nitride film and first oxide film. A second gate electrode of a second IGFET in the second region having a second lower layer electrode formed on a second gate insulating film and a second upper layer electrode formed on the second lower layer electrode. A second cap film is on the second upper layer electrode. A third nitride film is on a side surface of the second upper layer electrode that does not cover the side surface of the second cap film. A second oxide film is on a side surface of the second lower layer electrode. A second etching stopper film includes a fourth nitride film formed on the outside of the third nitride film and second oxide film. The first IGFET includes a lightly doped drain and the second IGFET does not include a lightly doped drain.

To address this rejection, the arguments set forth above with respect to claim 1 are incorporated herein by reference. Namely, the motivation to combine does not exist because there is no motivation to use *Kim et al.* to prevent an effect admitted not to exist in the reference being modified *Hung et al.*

Claims 22-24 have also been rejected based on *Hung et al.* in view of *Kim et al.* however there has been no mention of claim 21, from which claims 22-24 depend. Therefore, this rejection of these claims is believed to be defective.

Rejection of Claims 5 and 25 Under 35 U.S.C. §103(a), based on *Hung et al.* and *Kim et al.* further in view of *Liaw* (U.S. Patent No. 6,448,140 B1).

Claim 5 depends from claim 2, which depends from claim 1. Claim 5 recites that an interlayer insulating film is formed to cover the gate electrode of the IGFET. A contact hole is opened in the interlayer insulating film to expose a source/drain region of the IGFET. A conductor fills the contact hole and is electrically connected with the source/drain region.

To the extent this rejection relies on *Hung et al.* in view of *Kim et al.*, the arguments set forth above with respect to claim 1 are incorporated herein by reference.

Claim 25, which depends from claim 21, recites that the first lower layer gate electrode has a greater length than the first upper layer gate electrode.

No grounds for rejection were presented for base claim 21 based on based on *Hung et al.* and/or *Kim et al.* Accordingly, the rejection of this claim is also defective.

For these reasons, these grounds for rejection are traversed.

Rejection of Claims 21-27 Under 35 U.S.C. §103, based on *Hung et al* in view of *Akatsu et al.* (U.S. Patent No. 6,281,084 B1).

The semiconductor device of claim 21 includes a first transistor formed in a first region. The first transistor includes a first upper layer gate electrode formed on and in electrical connection with a first corresponding lower layer gate electrode. A first insulating film is formed on a majority of a side surface of the first lower layer gate electrode. A second insulating film is formed on a side surface of the first upper layer gate electrode. The second insulating film has a lower thermal growth rate with respect to the first upper layer gate electrode material than the thermal growth rate of the first insulating film with respect to the first lower layer gate electrode material. A first etching stopper film is formed on the outside of the first and second insulating films and in contact with a majority of an outside surface of the first insulating film formed on the majority of the side surface of the first lower layer gate electrode. The second insulating film has a thickness of less than 6 nm.

The rejection admits that *Hung et al.* does not disclose a "first etching stopper film in contact with a majority of an outside surface of the first insulating film formed on the majority of

the side surface of the first lower layer gate electrode", as recited in claim 21.[4]

To show such a limitation, the rejection relies on *Akatsu et al.*:

> However, Akatsu discloses... the etching stop film 30... (Office Action, dated 07/26/2005, Page 7, Lines 15-17).

Applicant must respectfully disagree with this interpretation of *Akatsu et al.* The film labelled 30 in *Akatsu et al.* is not an "etching stop film", as argued. In *Akatsu et al.*, film 30 is a thin barrier layer 30 of dielectric material:

> A thin barrier layer 30 of dielectric material is deposited over the semiconductor device 10. Particularly, the layer 30 is deposited over the semiconductor substrate oxide layer 16 and the gate stack 12. (*Akatsu et al.*, Col. 2, Lines 63-67).

Thin barrier layer 30 is a barrier layer to prevent impurity diffusion into the gate structure (such as impurities from second layer 32).

Thin barrier layer 30 is never used to stop an etch, and thus cannot be an etching stopper film. In fact the reference clearly teaches the exact opposite by etching through layer 30 to stop at a lower oxide layer:

> Particularly, the doped glass layer 32 is ***etched through the nitride layer 30*** and stopping selectively at the gate oxide layer 16. (*Akatsu et al.*, Col. 3, Lines 19-21).

Therefore, the layer 30 of *Akatsu et al.* cannot be considered to show or suggest the etching stopper film of claim 21.

Accordingly, because the combination of references *Hung et al.* and *Akatsu et al.* do not show all elements of amended claim 21, this ground of rejection is believed to be traversed.

[4] See the Office Action, dated 07/26/05, Page 7, Lines 12-14.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Claim 20 has been amended not in response to the cited art, but to address a typographical error.

The present claims 1-3, 5-7, and 17-28 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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Darryl G. Walker
Attorney
Reg. No. 43,232

Darryl G. Walker
WALKER & SAKO, LLP
300 South First Street
Suite 235
San Jose, CA 95113
Tel. 1-408-289-5314